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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/017,198	12/18/2001	Yuki Kondoh	HITA.0142	6344

7590 09/21/2004

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EXAMINER	
GERSTL, SHANE F	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 09/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/017,198	KONDOH ET AL.	
	Examiner	Art Unit	
	Shane F Gerstl	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 February 2002 and 18 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,12 and 13* is/are rejected.

7)☒ Claim(s) *11,14 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 December 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/18/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-15 have been examined.

Papers Received

2. Receipt is acknowledged of declaration and application papers submitted, where the papers have been placed of record in the file.

Drawings

3. Figures 1-4 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. This designation of prior art is supported by Applicant's specification, which describes the details of figures 1-4 in the background section. See MPEP § 608.02(g).

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: 313 and 513.

5. The drawings are objected to because the unlabeled rectangular boxes shown in the drawings must be provided with descriptive text labels for necessary understanding of the drawings pursuant to 37 CFR 1.84(o).

6. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet,

and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

7. Claim 12 is objected to because of the following informalities: the claim reads "...calculating a the semiABS..." but should read "...calculating the semiABS..." for grammatical correctness.

Appropriate correction is required.

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-6, 10, and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Blomgren (5,608,886).

10. In regard to claim 1, Blomgren discloses a processor (figure 6) comprising:

a. an instruction fetching circuit for calculating a lower portion of an effective address for an instruction word with a displacement, for replacing a value of the

displacement in the instruction word according to the calculating result, and for storing the value in a storage circuit; [Column 11, lines 10-22 show that a displacement is indicated by a branch opcode in an instruction word and is used to calculate a predicted target address, the lower bits of which are written as a target sub-address to a target finder array (figures 2 and 6, element 22) of an instruction cache. Column 6, lines 14-15 further show that this target sub-address is the lower portion of the predicted or effective target address. This sub-address that is used as the lower part or displacement of the effective address therefore replaces the opcode displacement when written into the finder array portion of the instruction cache.]

b. and the storage circuit for temporarily storing the instruction word, from which the stored instruction word is read at an instruction execution time, [Figure 2 and column 5, lines 11-30 show that the instruction cache stores the instructions words for further execution as shown in figure 6.]

c. wherein the effective address of said instruction word in the storage circuit is specified relative to a current value of a program counter address at the instruction execution time with the displacement, [Column 9, lines 2-12 and the sections above show that the effective address is specified relative to the address of the branch instruction of a PowerPC or x86 instruction set architecture. The architectures inherently have a program counter to specify this current branch instruction (or sequential instruction from the branch) to displace from.]

d. and wherein said processor utilizes the value stored in said storage as a lower portion of the effective address at the instruction execution time (as shown above).

11. In regard to claim 2, Blomgren discloses the processor of claim 1,

a. wherein said storage circuit has additional storage areas each of which one-on-one corresponds to each said instruction word,

b. and wherein said storage circuit stores the calculating result in said additional storage areas.

[Figure 2 along with the sections cited above show that the cache storage circuit contains a finder array that stores the calculated result in a an entry with a one-on-one correspondence with the instruction word and a tag.]

12. In regard to claim 3, Blomgren discloses the processor of claim 1, wherein the effective address is a branch target address (as shown above).

13. In regard to claim 4, Blomgren discloses the processor of claim 2, wherein the effective address is a branch target address (as shown above).

14. In regard to claim 5, Blomgren discloses the processor of claim 1, wherein said storage circuit is a cache or a buffer (as shown above).

15. In regard to claim 6, Blomgren discloses a processor (figure 6) comprising:

a. a storage circuit for temporarily storing an instruction word, from which the stored instruction word is read at an instruction execution time; [Figure 2 and column 5, lines 11-30 show that the instruction cache stores instructions words for further execution as shown in figure 6.]

b. a decoder for receiving the instruction word and for determining whether an effective address of said instruction word is specified as a PC relative displacement value; [Column 10, line 63 – column 11, line 4 show that a finder decoder decodes the instruction words and determines if a branch is specified. Column 9, lines 2-12 and the sections above show that an effective address is specified relative to the address of the branch instruction of a PowerPC or x86 instruction set architecture. The architectures inherently have a program counter to specify this current branch instruction (or sequential instruction from the branch) to displace from.]

c. an adder for adding of the PC relative displacement value and predetermined lower bits of the PC address, and for outputting the calculating result as a portion of the effective address if said instruction word has the PC relative displacement value; [Column 11, lines 5-22 show that an opcode displacement and the current address (PC) calculate a predicted effective address if there is a branch and output the lower portion of it for storage.]

d. and a selector for replacing the displacement value in the instruction word with the calculating result outputted from said adder, and for outputting said replaced result to said storage circuit as a semiABS displacement value of the instruction, if said instruction word has the PC relative displacement value. [Column 6, lines 14-15 further show that this predicted address is the lower portion of the predicted or effective target address. This sub-address that is used as the lower part or displacement of the effective address therefore replaces the

opcode displacement when written into the finder array portion of the instruction cache. The address is selected for entry into the cache by this selection circuitry. Figure 4 shows that this address is then used as a semi absolute (semiABS) address since it is directly used as a portion of the address for branching as is the definition in the specification.]

16. In regard to claim 10, Blomgren discloses the processor of claim 6, wherein said storage circuit is an instruction cache (as shown above).

17. In regard to claim 12, Blomgren discloses a method for converting a first instruction word with a PC relative displacement value into a second instruction word with a semiABS displacement value, comprising:

a. calculating a the semiABS displacement value by adding predetermined lower bits of a PC address and the PC relative displacement value; [Column 11, lines 5-22 show that a current address (the PC since either an x86 or PowerPC architecture is used as shown in column 9, lines 2-12) is added to an opcode displacement, which is then used as a predicted target sub-address, which is a semiABS address as shown in figure 4 since it is a direct displacement portion of the address to branch to (element 40) as is consistent with the definition in the specification.]

b. replacing the PC relative displacement value in the first instruction word with the calculating result (as shown above);

c. and storing the second instruction word with the semiABS displacement value in a storage circuit (the cache of figure 2),

d. whereby the semiABS displacement value stored in said storage circuit is then immediately used as a portion of an effective address at the instruction execution time (as shown in figure 4).

Claim Rejections - 35 USC § 103

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

19. Claims 7-9 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blomgren.

20. In regard to claim 7,

a. Blomgren discloses the processor of claim 6, further comprising an effective address calculator for receiving a portion of the instruction word that has been stored in said storage circuit, and for calculating the effective address by using the semiABS displacement value at the instruction execution time.

b. Blomgren does not explicitly disclose performing a sign bit extension on the effective address.

c. The examiner is taking official notice that it would have been obvious to one of ordinary skill in the art at the time of invention modify the design of Blomgren to sign extend the value received by or output by the multiplexer of figure 4 (element 42) so that all 23 bits of the upper portion of the effective address are known and controlled.

21. In regard to claim 8,

a. Blomgren discloses the processor of claim 6,

b. Blomgren does not explicitly disclose wherein said storage circuit includes an area for storing a carry bit from said adder corresponding to the instruction word.

c. There will be times when the adder generates a carry bit. As shown in column 6, line 34 – column 7, line 3, there is a 2-bit type field in the cache indicating which block of instruction memory will be branched to (current, previous, or next).

d. The examiner is taking official notice that it would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Blomgren to base this type field on the carry from the adder since this carry already indicates if an address is too high or low for a current memory block and it would be very convenient to use this data. A positive carry would be used to generate the value "01" to indicate the next block, "10" to indicate the previous, and "00" if there is no carry and the current block is used all as indicated in the table of column 6.

22. In regard to claim 9,

a. Blomgren discloses the processor of claim 8,

i. further comprising: an effective address calculator for receiving a portion of the instruction word that has been stored in said storage circuit (figure 4, element 80), and for calculating the effective address with the

semiABS displacement value at the instruction execution time (as shown above using element 40 of figure 4),

ii. wherein said effective address calculator calculates said effective address by using the carry bit stored in said storage circuit (of field 31 of figure 4).

b. Blomgren does not explicitly disclose performing a sign bit extension of the received portion.

c. The examiner is taking official notice that it would have been obvious to one of ordinary skill in the art at the time of invention modify the design of Blomgren to sign extend the value received by or output by the multiplexer of figure 4 (element 42) so that all 23 bits of the upper portion of the effective address are known and controlled. This would be done with the carry bit from the adding result in the sense that the multiplexer result depends on the carry bits.

23. In regard to claim 13,

a. Blomgren discloses the method according to claim 12, further comprising:

i. receiving a portion of the instruction word stored in said storage circuit; [Figure 4 shows element 80 receiving a portion of the stored word.]

ii. and calculating the effective address with the semiABS displacement value at the instruction execution time (as shown above).

b. Blomgren does not explicitly disclose performing a sign bit extension without using a carry bit carried from the adding result.

c. The examiner is taking official notice that it would have been obvious to one of ordinary skill in the art at the time of invention modify the design of Blomgren to sign extend the value received by or output by the multiplexer of figure 4 (element 42) so that all 23 bits of the upper portion of the effective address are known and controlled. This would be done without a carry bit from the adding result since the sign extension itself should be done to the values (such as "0" of figure 4) regardless of the carry.

Allowable Subject Matter

24. Claim 11 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record does not specifically disclose an apparatus for recovering a disregarded carry bit generated during the method according to claim 6, including: a comparator for comparing the semiABS displacement value and lower bits of the PC address and a decoder for receiving the comparing result, a sign_bit of the semiABS displacement value, and a bit which is a digit higher than the highest bit of the lower bits of the PC address in the PC address thereby outputting a selecting signal for selecting one of +1, 0, and -1 according to a predetermined conversion table. Further, no prior art of record suggests that it would have been obvious to modify the disclosure to include an apparatus for recovering a disregarded carry bit generated during the method according to claim 6, including: a comparator for comparing the semiABS displacement value and lower bits of the PC address and a decoder for receiving the comparing result, a sign_bit of the semiABS

displacement value, and a bit which is a digit higher than the highest bit of the lower bits of the PC address in the PC address thereby outputting a selecting signal for selecting one of +1, 0, and -1 according to a predetermined conversion table.

25. Claim 14 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record does not specifically disclose a method for recovering a disregarded carry bit generated during the method according to claim 13, including: comparing the semiABS displacement value and lower bits of the PC address; receiving the comparing result, a sign bit of the semiABS displacement value, and a bit which is a digit higher than the highest hit of the lower bits of the PC address in the PC address thereby outputting a selecting signal for selecting one of +1, 0, and -1 according to a predetermined conversion table; and adding +1, 0, or -1 to the rest bits of the PC address then to a upper portion of the effective address with a bit number equal to the rest bits of the PC address according to the selecting signal thereby recovering a carry bit carried from the most significant bit of the add step. Further, no prior art of record suggests that it would have been obvious to modify the disclosure to include a method for recovering a disregarded carry bit generated during the method according to claim 13, including: comparing the semiABS displacement value and lower bits of the PC address; receiving the comparing result, a sign bit of the semiABS displacement value, and a bit which is a digit higher than the highest hit of the lower bits of the PC address in the PC address thereby outputting a selecting signal for selecting one of +1, 0, and -1 according to a predetermined conversion table; and

adding +1, 0, or -1 to the rest bits of the PC address then to a upper portion of the effective address with a bit number equal to the rest bits of the PC address according to the selecting signal thereby recovering a carry bit carried from the most significant bit of the add step.

26. Claim 15 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record does not specifically disclose a method for recovering a disregarded carry bit generated during the method according to claim 13, including: comparing the semiABS displacement value and lower bits of the PC address to obtain a carry bit carried from the adding step; performing an exclusive OR operation on the carry bit, a sign bit of the semiABS displacement value, and the bit which is a digit higher than the highest hit of the lower bits of the PC address in the PC address thereby outputting a sign bit of the PC relative displacement value of the first instruction word; and adding the carry bit, the sign bit, and the bit which is a digit higher than the highest hit of the lower bits of the PC address in the PC address to recover a carry bit carried from the adding step. Further, no prior art of record suggests that it would have been obvious to modify the disclosure to include a method for recovering a disregarded carry bit generated during the method according to claim 13, including: comparing the semiABS displacement value and lower bits of the PC address to obtain a carry bit carried from the adding step; performing an exclusive OR operation on the carry bit, a sign bit of the semiABS displacement value, and the bit which is a digit higher than the highest hit of the lower bits of the PC address in the PC address

thereby outputting a sign bit of the PC relative displacement value of the first instruction word; and adding the carry bit, the sign bit, and the bit which is a digit higher than the highest hit of the lower bits of the PC address in the PC address to recover a carry bit carried from the adding step.

Conclusion

27. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

28. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following references further show the art with respect to branch calculation and predecoded storage in general.

US Pat No 6,502,185 to Keller teaches a predecode cache for analyzing data of instructions before they are fetched. The reference also teaches in the background that this predecoding has typically been done within the instruction cache or with a one-on-one mapping to the instruction cache so that the actual words are modified.

US Pat No 6,044,455 discloses a predecoding mechanism for identifying an address mode such as adding the PC to an immediate value.

US Pat No 6,243,805 to Mahurin shows how to predecode instructions including conditional branch instructions and use the program counter and target address.

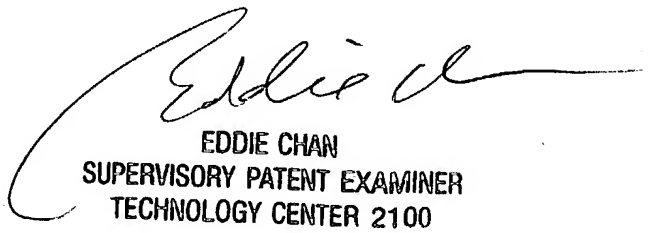
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane F Gerstl whose telephone number is (571) 272-4166 after October 12 and (703) 305-7305 before October 12. The examiner can normally be reached on M-F 6:45-4:15 (First Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162 after October 12 and (703) 305-7305 before October 12. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shane F Gerstl
Examiner
Art Unit 2183

SFG
September 17, 2004



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